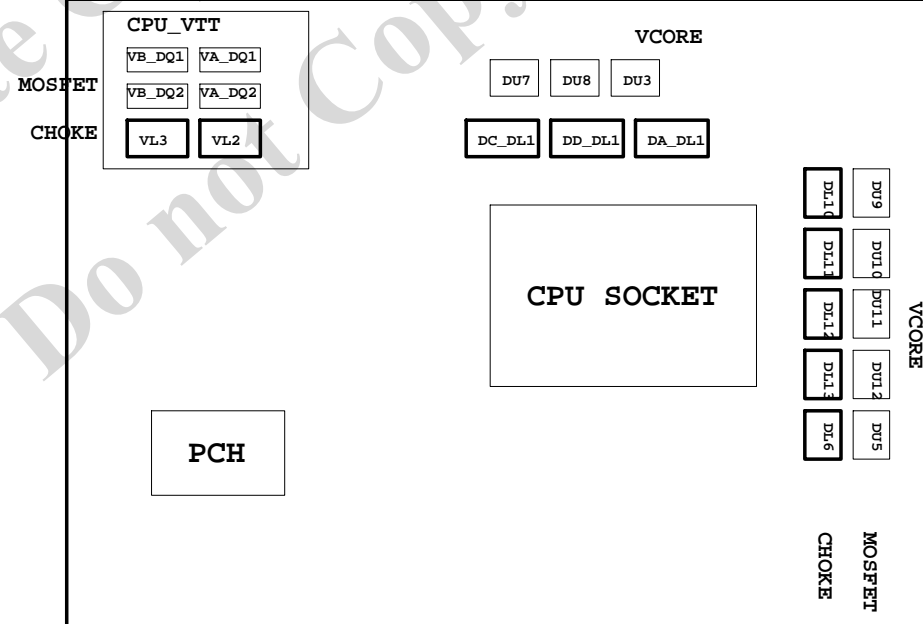


SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*4 SLOT
19	IT8892
20	PCI SLOT 1
21	HDMI/DVI/USB3.0
22	MSATA
23	Dual BIOS / TPM CONNECT
24	ALC889
25	REAR AUDIO JACK
26	VCORE PWM_IR3567
27	VCORE PWM_IR3567

28	VCORE PWM_IR3570
29	DDR / CPU_VTT MOS
30	DISCRETE POWER
31	VCCSA POWER
32	I/O ITE8728
33	COM,-PHOT,RUSB
34	FP,FUSB
35	ATX POWER, CLOCK GEN
36	HWM,KB/MS , FAN CTRL
37	ARTHEROS AR8161/AR8151
38	MARVELL 9172
39	NCT3933U
40	VIA VL800 USB3.0
41	TABLE LIST



Gigabyte Technology

GA-Z77X-D3H

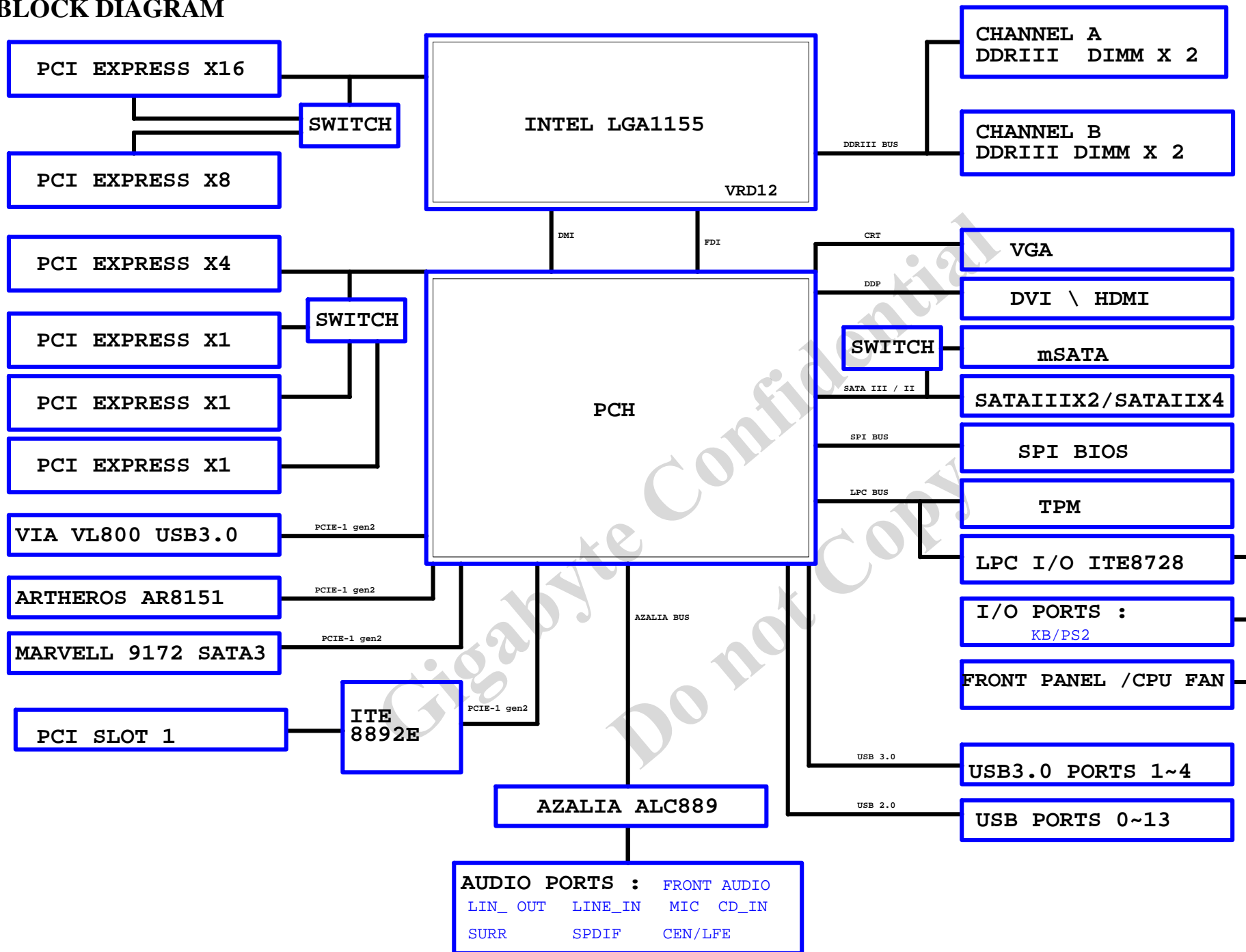
Component value change history

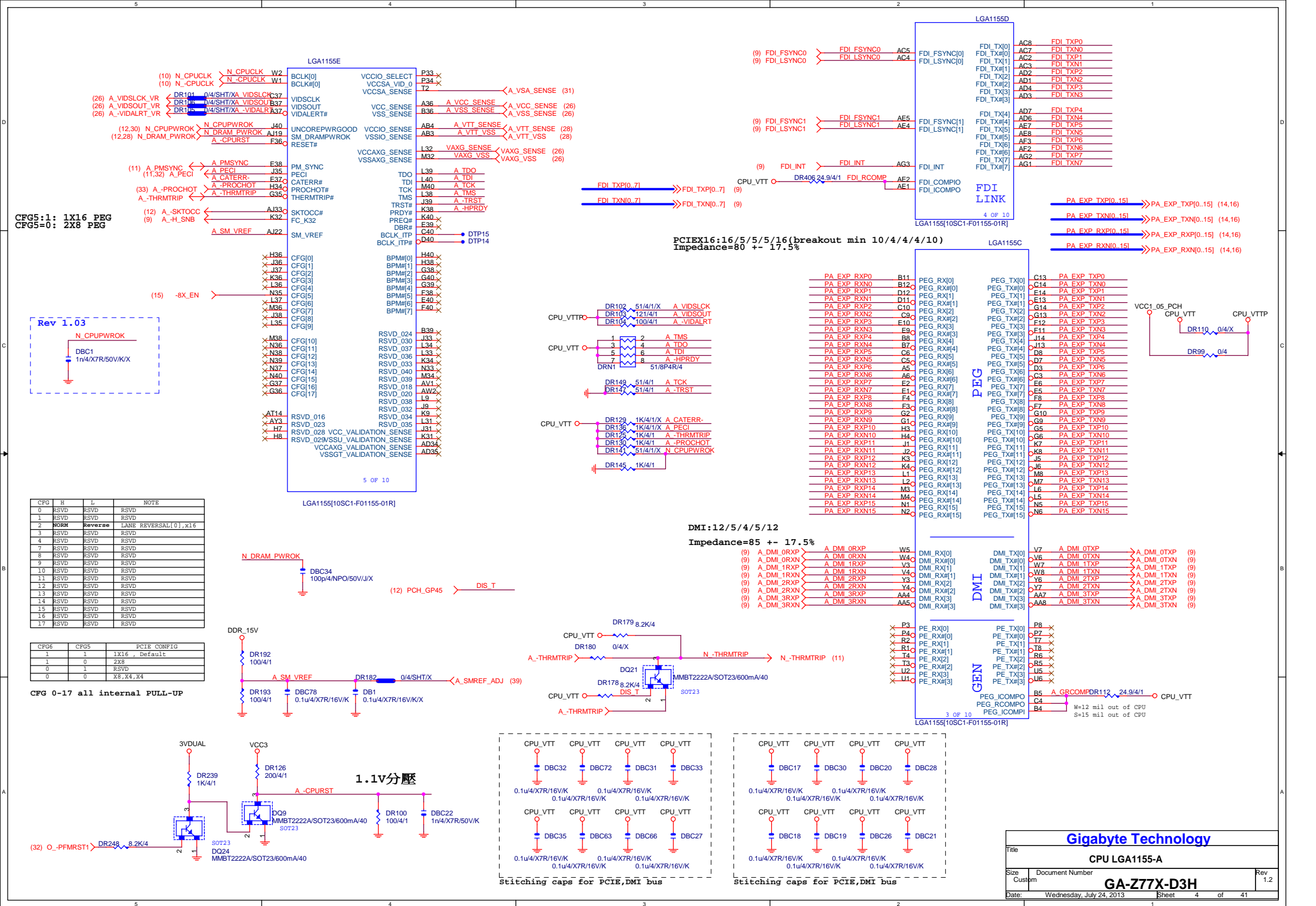
Data	Change Item	Reason
2011/12/02	1.First BOM. (GA-Z77X-D3H-01_20111125_1000-BOM.DSN)	
2012/01/03	1.PCH==>10HB1-030Z77-10R 2.PCH_HS==>12SP2-S05511-01R 3.ADD NR100 4.EMI ADD BC330 5.ADD PI3PCIE2415 FOR PCIEX4 SW TO X1 6.REMOVE DUAL BIOS SW 7.AUDIO CONNECT CHANGE TO 11NR6-403025-61R 8.REMOVE SURR BACK 9.DRAT2,DART3,MART3==>47K/1/4/S 10.DAR44,DAR15,MAR185==>0 OHM 11.ADD VA_DR2 FOR漏電 12.REMOVE DA_Q2,DB_DQ2==>DA_DQ3,DB_DQ3 13.後窗USB/USB_LAN CONNECT CHANGE TO USB3.0	9MZ77XD3H-00-02
2012/01/13	Modify 1.MAR149,DAR51,DAR1,24.9/4/1變更為'100/4/1 2.DART2,DART3,MART3,47K/1/4/S變更為47K/1/4/S/[10RH3-004702-21R] 3.MAC361,DAC24,DAC1,1N/4/X7R/50V/K變更為3.3n/4/X7R/50V/K 4.MAR151,DAR54,DAR2,24.9/4/1變更為0/4 Add 5..R5409,R5413,10K/4/1 6.R5412,R5408,45.3K/4/1 7.DAR82,0/4 8.C2068,C2069,0.1u/4/X7R/16V/K 9.Q668,Q670,2N7002/SOT23/25pF/5 10.U219,LM358DR/SO8 11.R5414,R5410,1.65K/4/1 12.RS1,RS2,100K/1/4/S 13.R_USB30_1,USB/18P/BU/OS/RA/D/2/HR 14.DB_DQ2,DA_DQ2,DF_DQ3,DE_DQ3,DD_DQ3,DC_DQ3,RJK0393DPA-0G/N/4.3m/PPAKSO-8 15.R5411,R5415,1K/4/1 16.RHC3,GBC28,LAC33,47p/4/NPO/50V/J Delete 1.UCR29,'8.2K/4 2.UCR25,'6.04K/4/1 3.UCQ2,'2N7002/SOT23/25pF/5 4.R_USB30,'USB/18P/BU/OS/RA/D/2/HR 5.U8,'NCT3931U-2/SOT23-8	9MZ77XD3H-00-10A
2012/01/13	1.DA_DR11,DC_DR11,DE_DR11,DZ_DR11,1/4 change to 0/4 2.FAN1/2/3 change to SYS_FAN1/2/3,V-A AMP WF 1*4P PINREX	9MZ77XD3H-00-10B
2012/01/31	1.R5410,R5414,1.65K change to 3.65K	9MZ77XD3H-00-10C
2012/02/03	Modify 1.R5410,'3.65K/4/1變更為'1.65K/4/1 2.DAR6,'5.36K/4/1變更為'5.1K/4/1 3.DY_DL1,DZ_DL1,VL2,DA_DL1,DB_DL1,DC_DL1,DE_DL1,DF_DL1, '0.8uH/35A/INC109/F/D變更為'0.36uH/38A/IGC109/FS/D 4.DAR45,DAR40,'1.54K/4/1變更為'1.74K/4/1 5.DAR5,DAR8,'4.12K/4/1變更為'4.75K/4/1 6.R5414,'3.65K/4/1變更為'2.49K/4/1 7.DAR13,DAR36,DAR25,DAR59,DAR62,DAR75,DAR21,2K/4/1變更為1.2K/4/1 8.DAR42,'2.05K/4/1變更為2.37K/4/1 Add 1.DZ_DR10,DE_DR10,DC_DR10,DA_DR10,'0/4 Delete 1.DE_DR11,DC_DR11,DA_DR11,DZ_DR11,'0/4	9MZ77XD3H-00-10D
2012/02/07	Modify 1.DAR6,5.1K/4/1 change to 5.49K/4/1	9MZ77XD3H-00-10E
2012/03/13	1.Add MR34,MR35==>0 ohm 2.Remove UCU1 VIA USB30 EEPROM 3.Delete OR48,Add OR51 for MB_ID3	9MZ77XD3H-00-10K
2012/03/22	1.Add UCU1 EEPROM	9MZ77XD3H-00-10L
2012/03/23	1.PCB change to 1.03	9MZ77XD3H-00-10Q

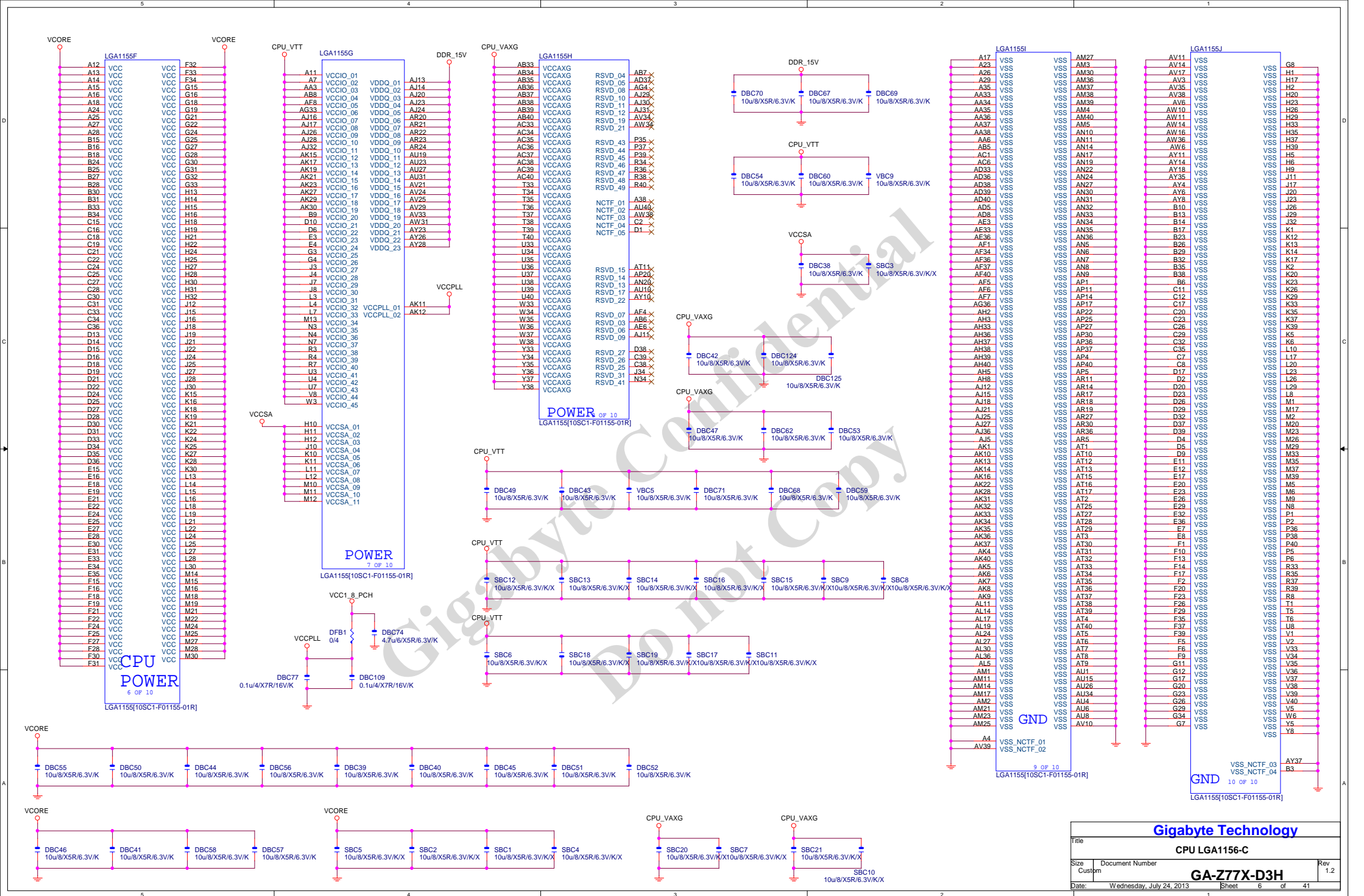
Circuit or PCB layout change

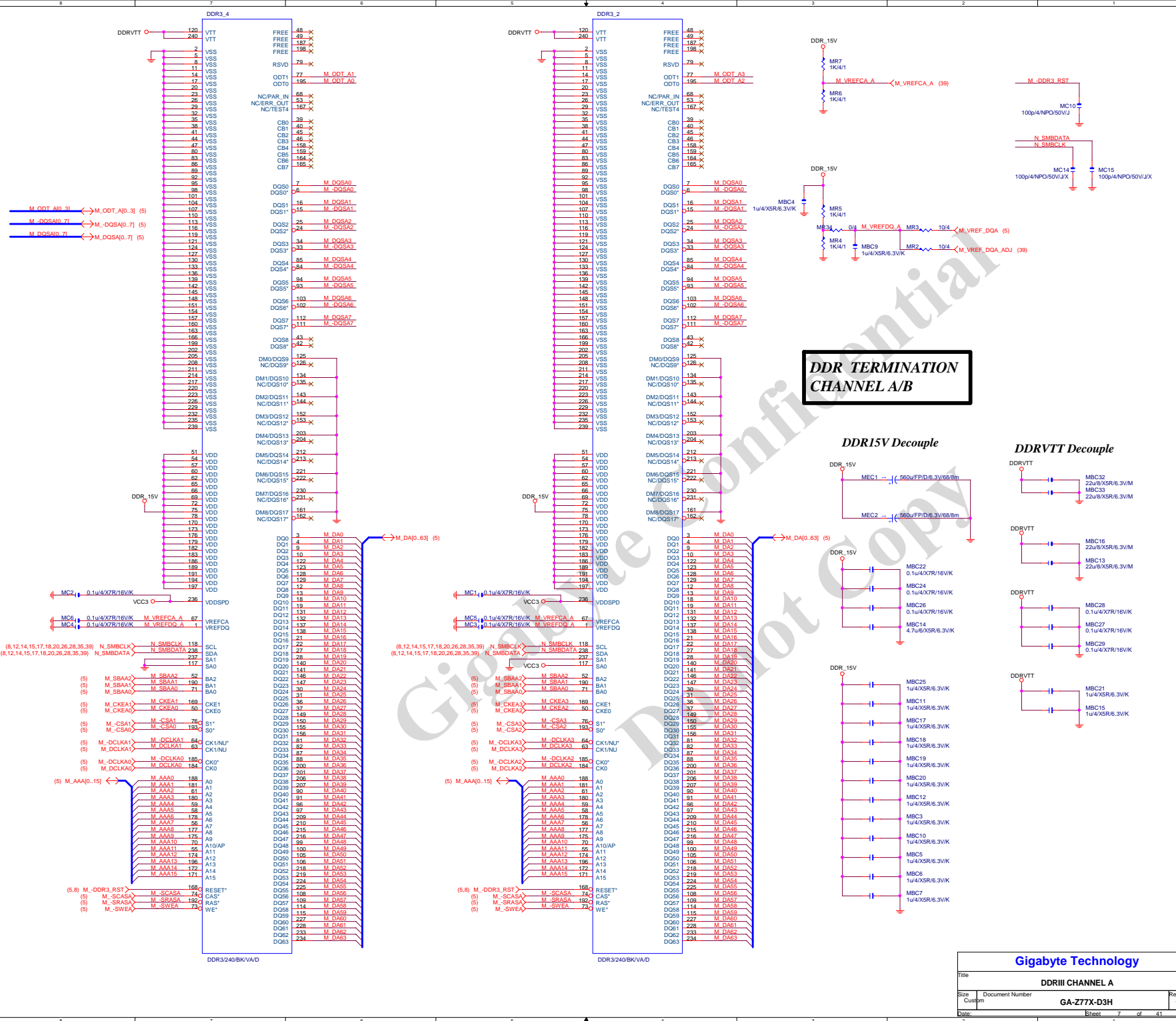
DATE	Change Item	Reason
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	(Change from Z77X-UD3H-01A_1124_EBOM.DSN)	
2012/01/02	1.PARN2 change to 0/8P4R/4/X 2.ADD PI3PCIE2415 FOR PCIEX4 SW TO X1 3.REMOVE DUAL BIOS SW 4.AUDIO CONNECT CHANGE TO 11NR6-403025-61R (WITH SPDIF) 5.REMOVE SURR BACK 6.CPU_VTT ADD DUAL POWER 防漏電 7.VL2轉方向 8.ADD VIA VL800 USB3.0 9.後窗USB/USB_LAN CONNECT CHANGE TO USB3.0 10.ADD ATX POWER LOAD RESISTOR 11.SYS_FAN1/2/3 RENAME TO FAN1/2/3	REV 0.2
2012/01/13	1.Add PWM 3VDUAL input 2.Add GBC28 3.Add 2組 VR_HOT control線路 4.DAR53,DAR55,MAR148 CHANGE TO R0402-2 5.R_USB30 rename to R_USB30_1	REV 1.0
2012/01/19	1.FAN1/2/3 rename to SYS_FAN1/2/3	Rev 1.01
2012/02/22	1.DDR T型走線 2.Add MR34,MR35	Rev 1.02
2012/03/21	1.縮短DDR slot 間距 for O.C. 2.Add DBC1 for EMI ESD improve	Rev 1.03
2012/05/28	1.版本改為 Rev 1.1 2.FB2,FB3,FB4, FB0603-RH change to FB0402-RH 3.msATA MINI_PCIE52P-A-1 change to MINI_PCIE52P-B-1-COLAY 4.ATX_12V change to ATX_12V_2X4 5.CFB1,FB6,NFB3,NFB4,NFB5,NFB6,LAFB2,LAFB3,RHFB2,change to 0402 6.Add R854,BC36	
2012/07/23	1. Rev 1.2 for remove Virtu MVP	Rev 1.2

BLOCK DIAGRAM



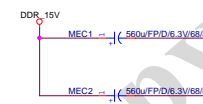




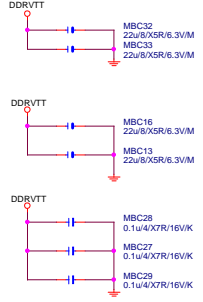


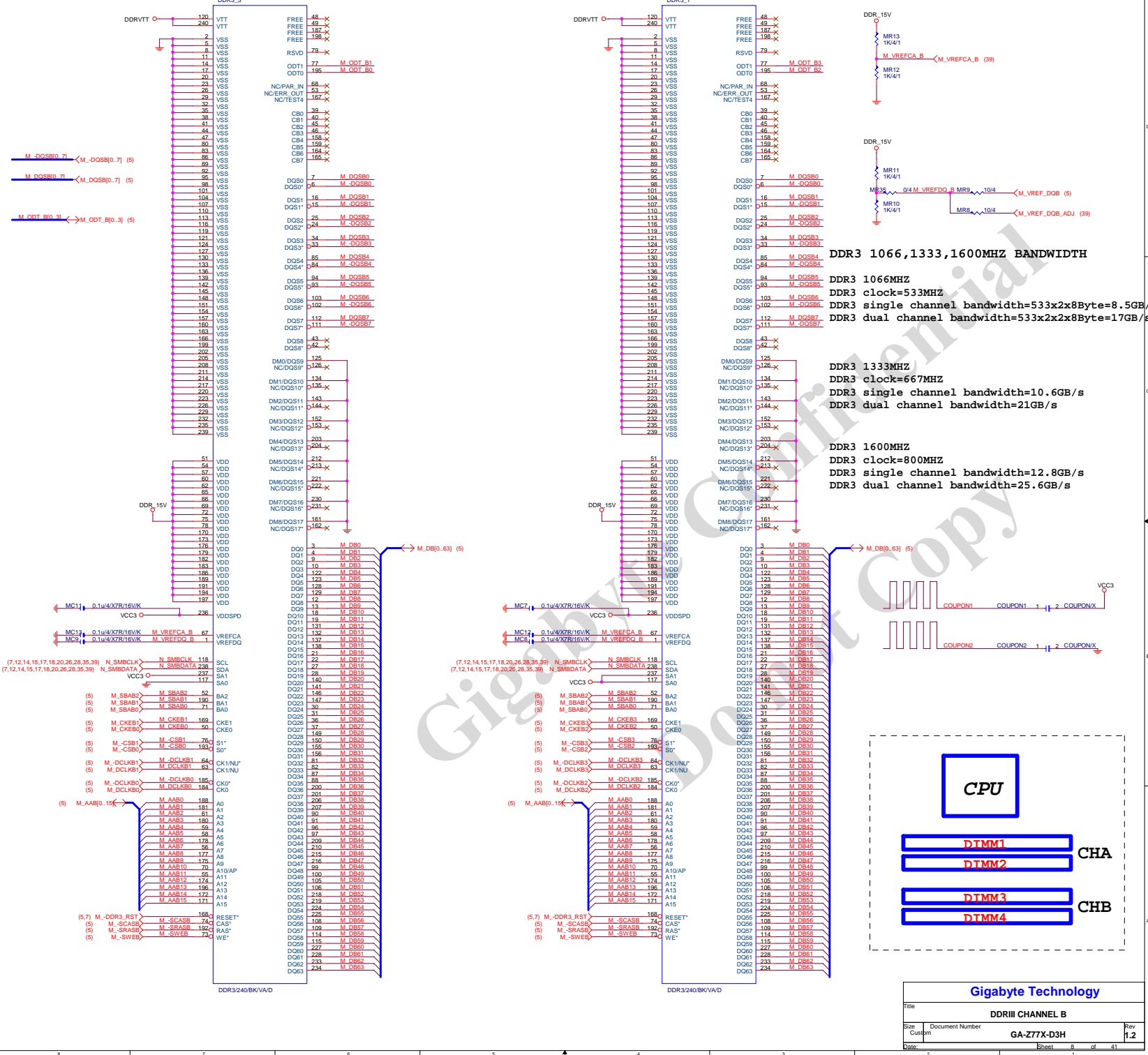
DDR TERMINATION
CHANNEL A/B

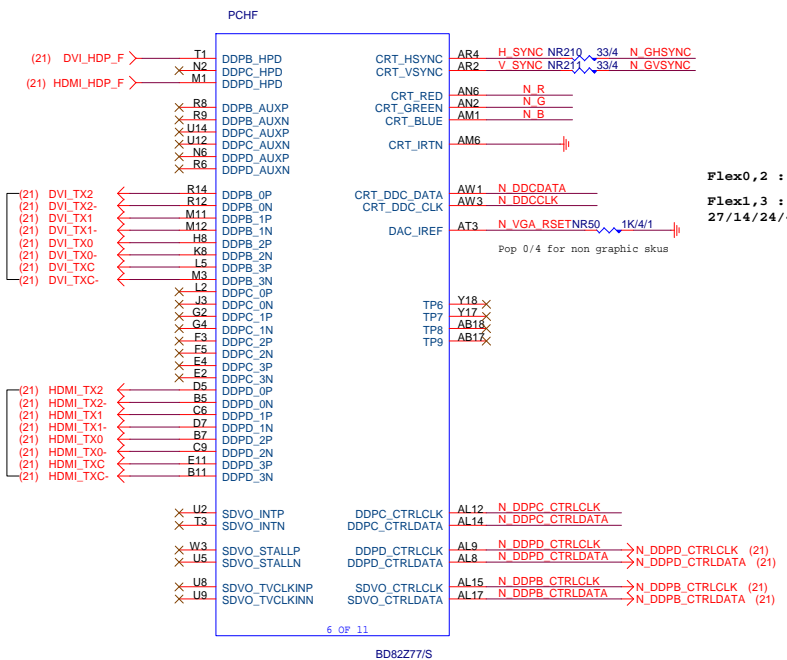
DDR15V Decouple



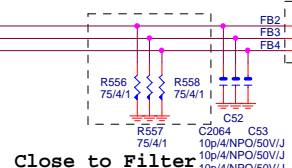
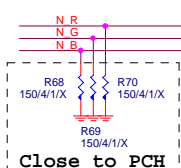
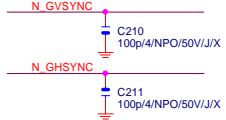
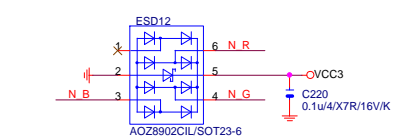
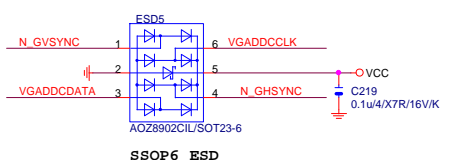
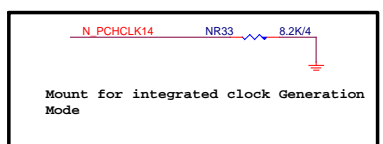
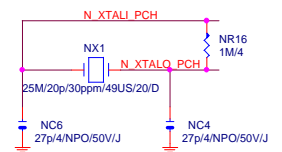
DDRVRTT Decouple



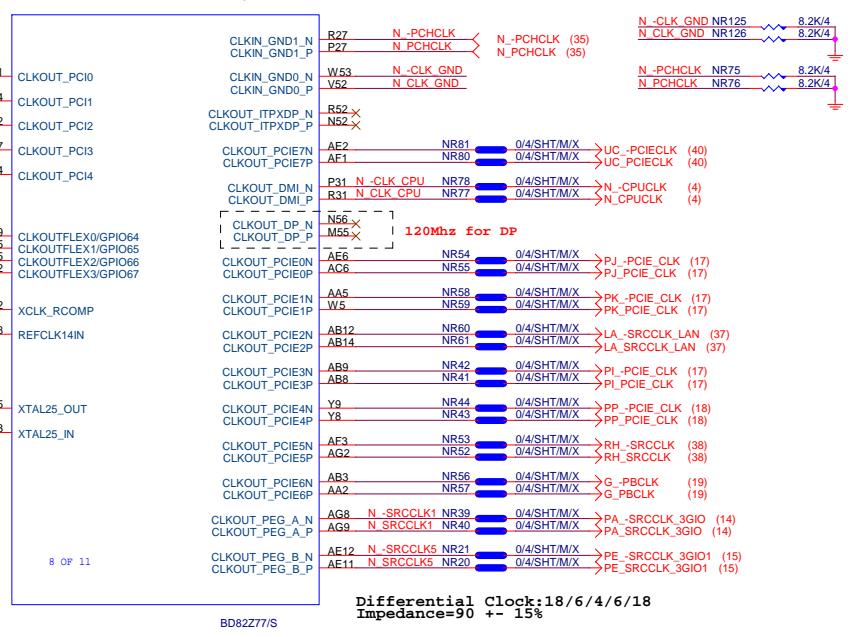




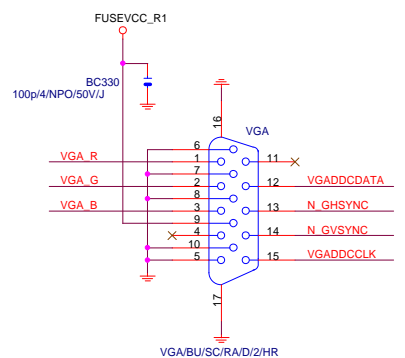
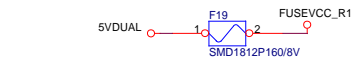
Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ



Rev 1.1



Differential Clock:18/6/4/6/18
Impedance=90 +- 15%



Gigabyte Technology			
PCH DISPLAY ,CLK BUFFER			
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SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

PCHC

PCHA

MB-ID

For WIFI

NR177

0/4/SHT/MX

N ME PWROK

NC19

0.01u/4/X7R/25V/K/X

N GPIO17

N GPIO1

N GPIO6

N PHASE_CTRL

N GPIO68

N GPIO69

N GPIO70

N GPIO71

(32) N_SSTCTL

NC43

CL_CLK1

CL_DATA1

CL_RST1#

APWROK

PWM0

PWM1

PWM2

PWM3

TACH0_GPIO17

TACH1_GPIO1

TACH2_GPIO6

TACH3_GPIO7

TACH4_GPIO68

TACH5_GPIO69

TACH6_GPIO70

TACH7_GPIO71

SST

SCLOCK/GPIO22

SLOAD/GPIO38

SDATAOUT0/GPIO39

SDATAOUT1/GPIO48

NC_5

AY20

NRN8

8.2K/8P4R/4

N GPIO70

N GPIO6

N GPIO17

N GPIO1

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

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NC43

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NC-219

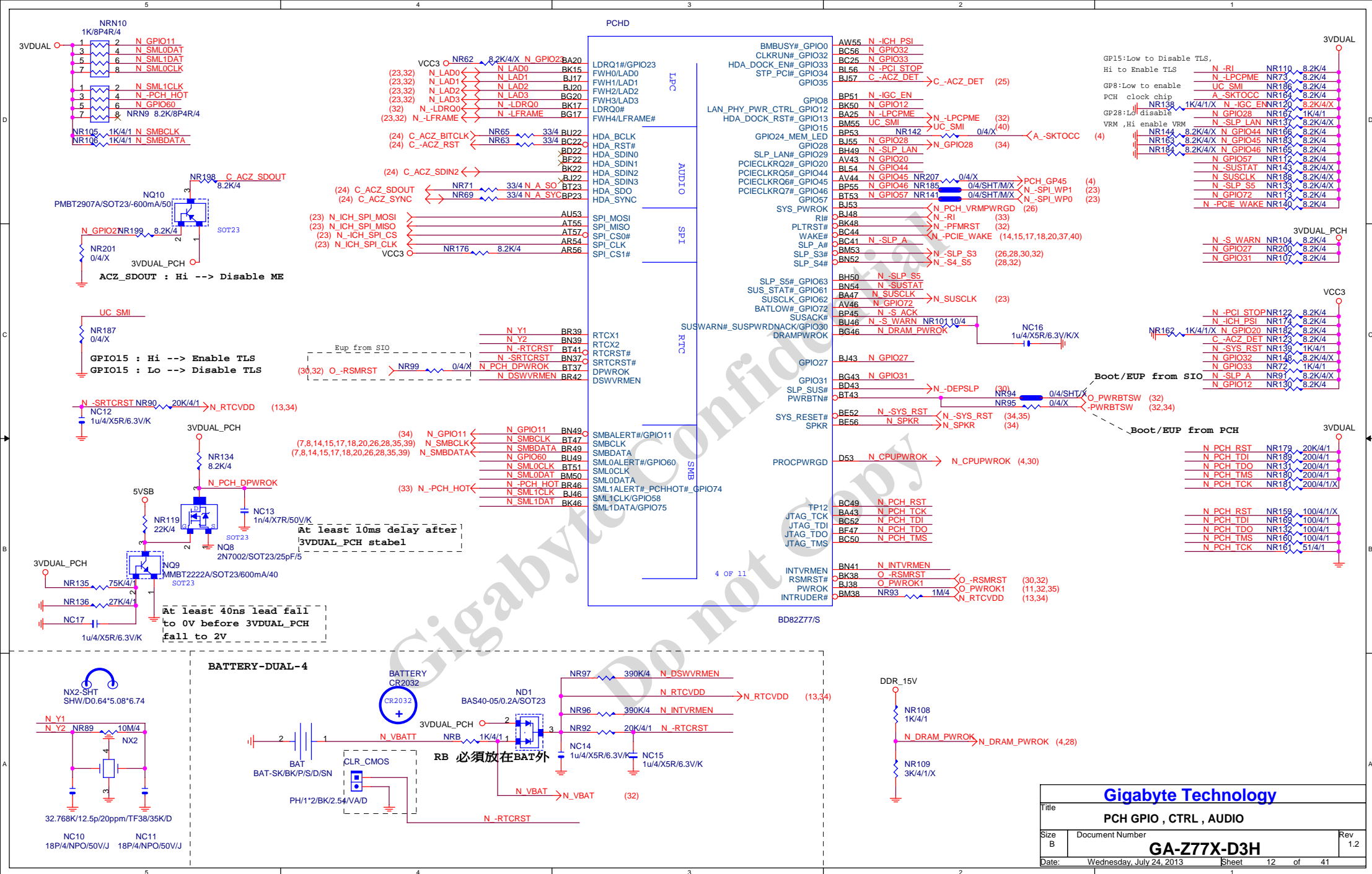
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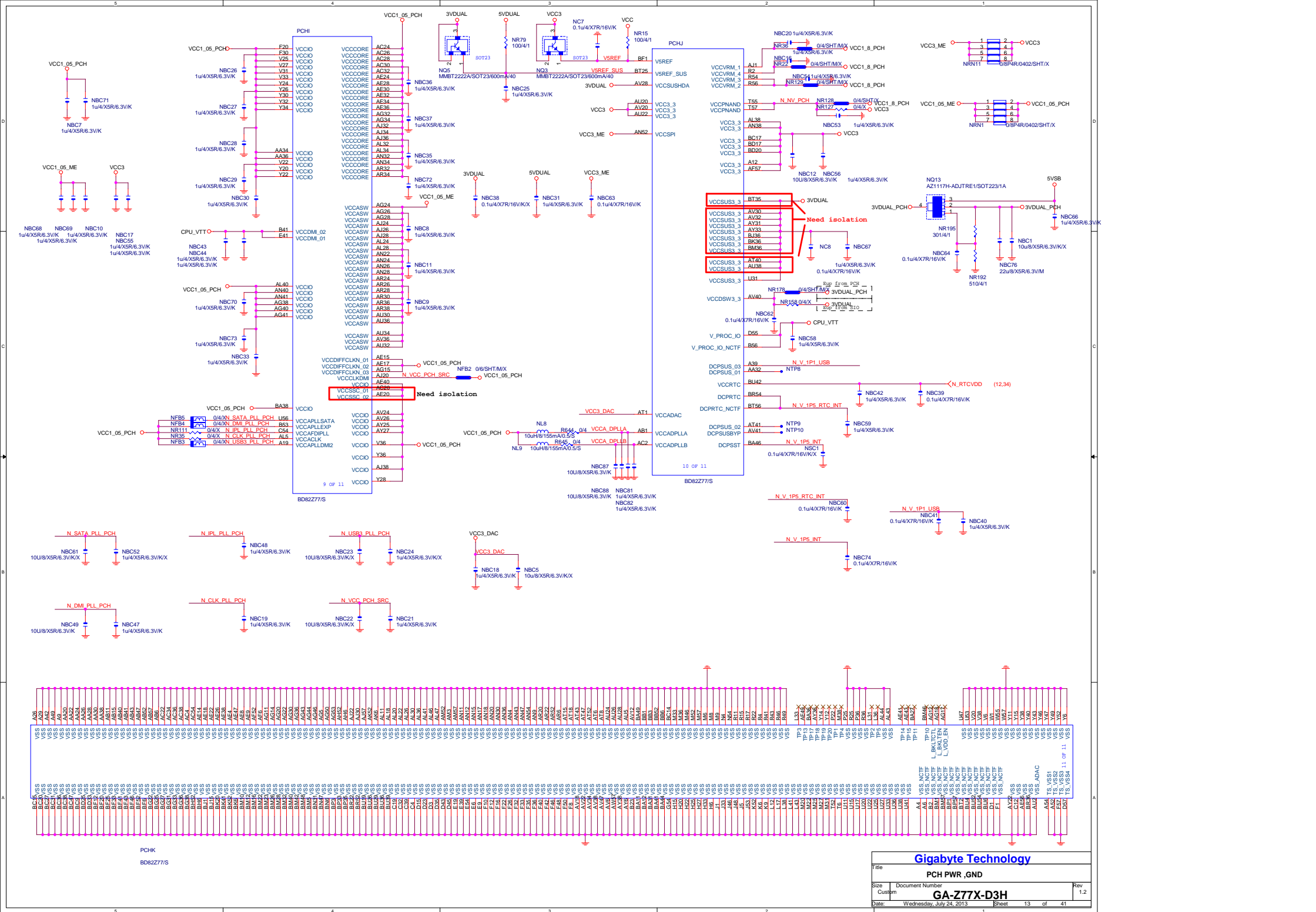
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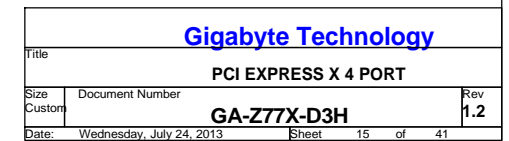
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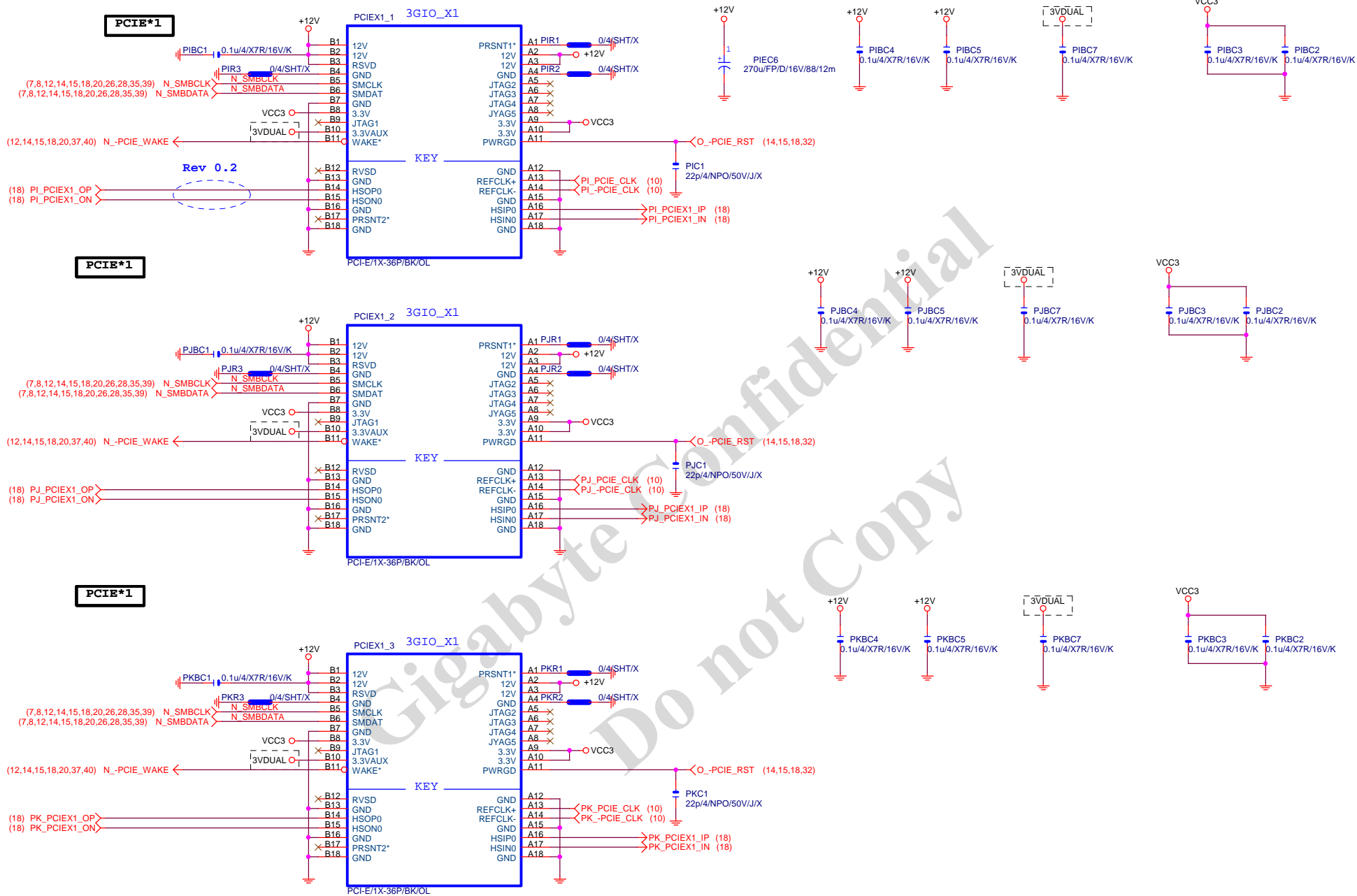
NC-223

NC-224





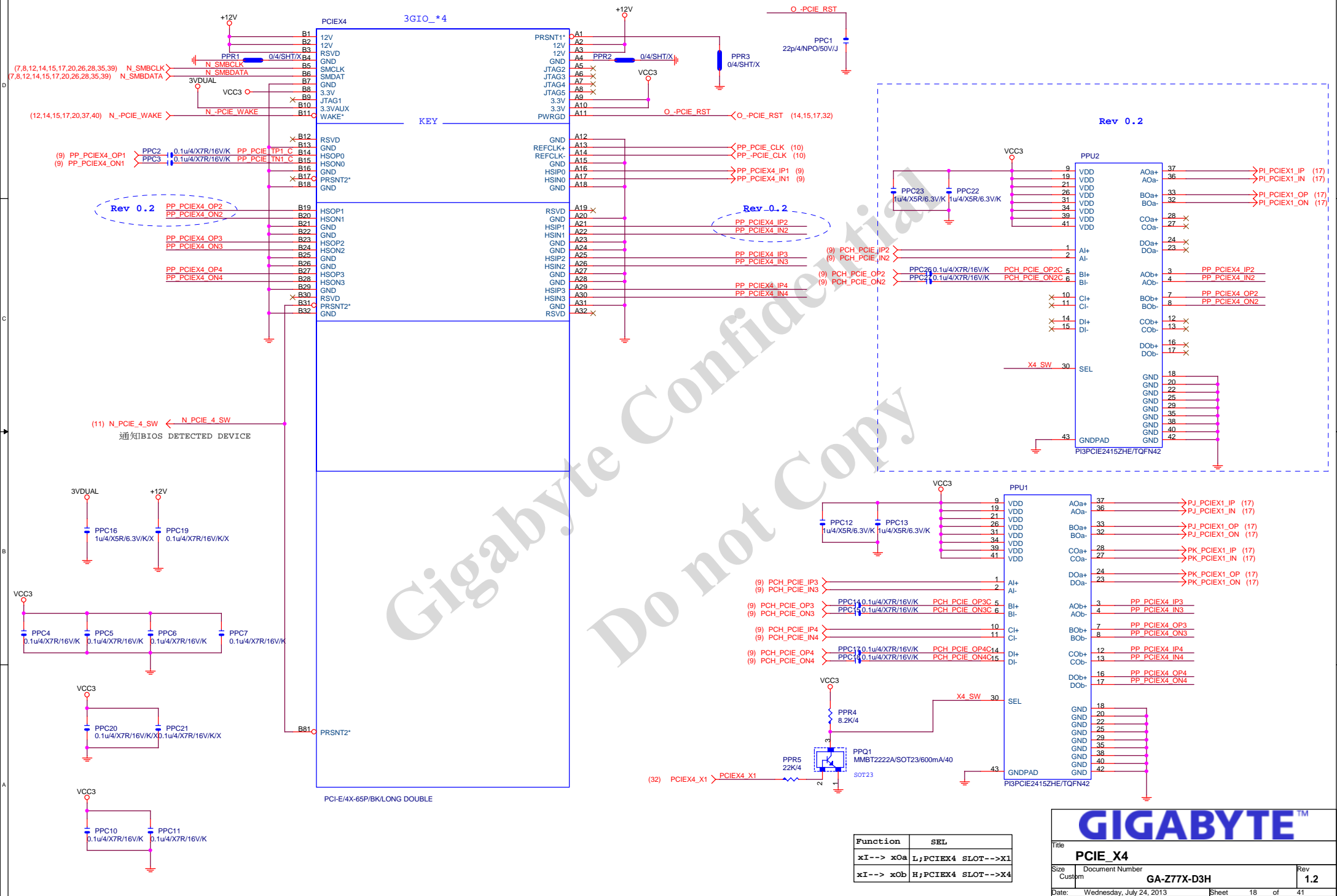


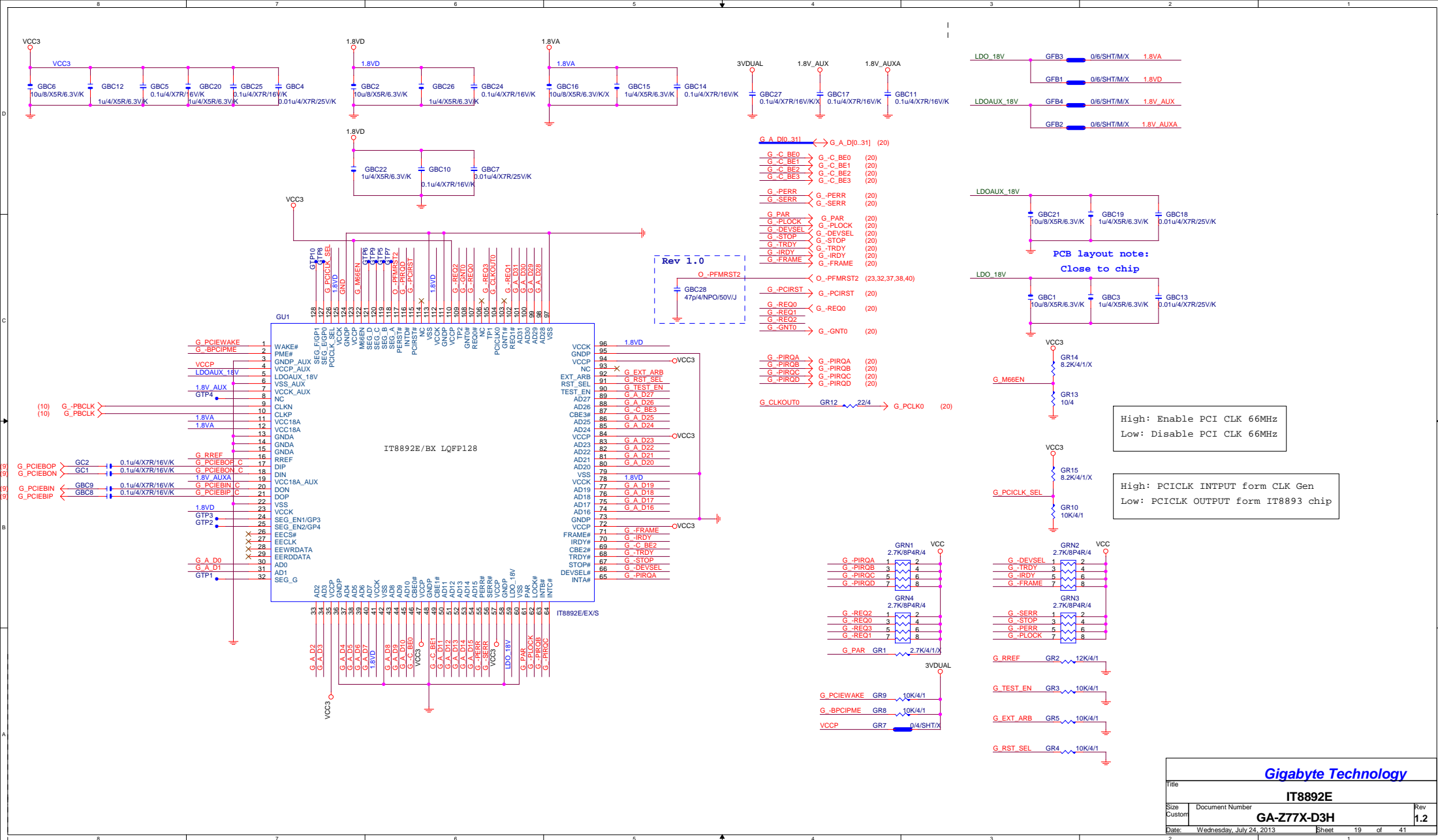


Gigabyte Technology

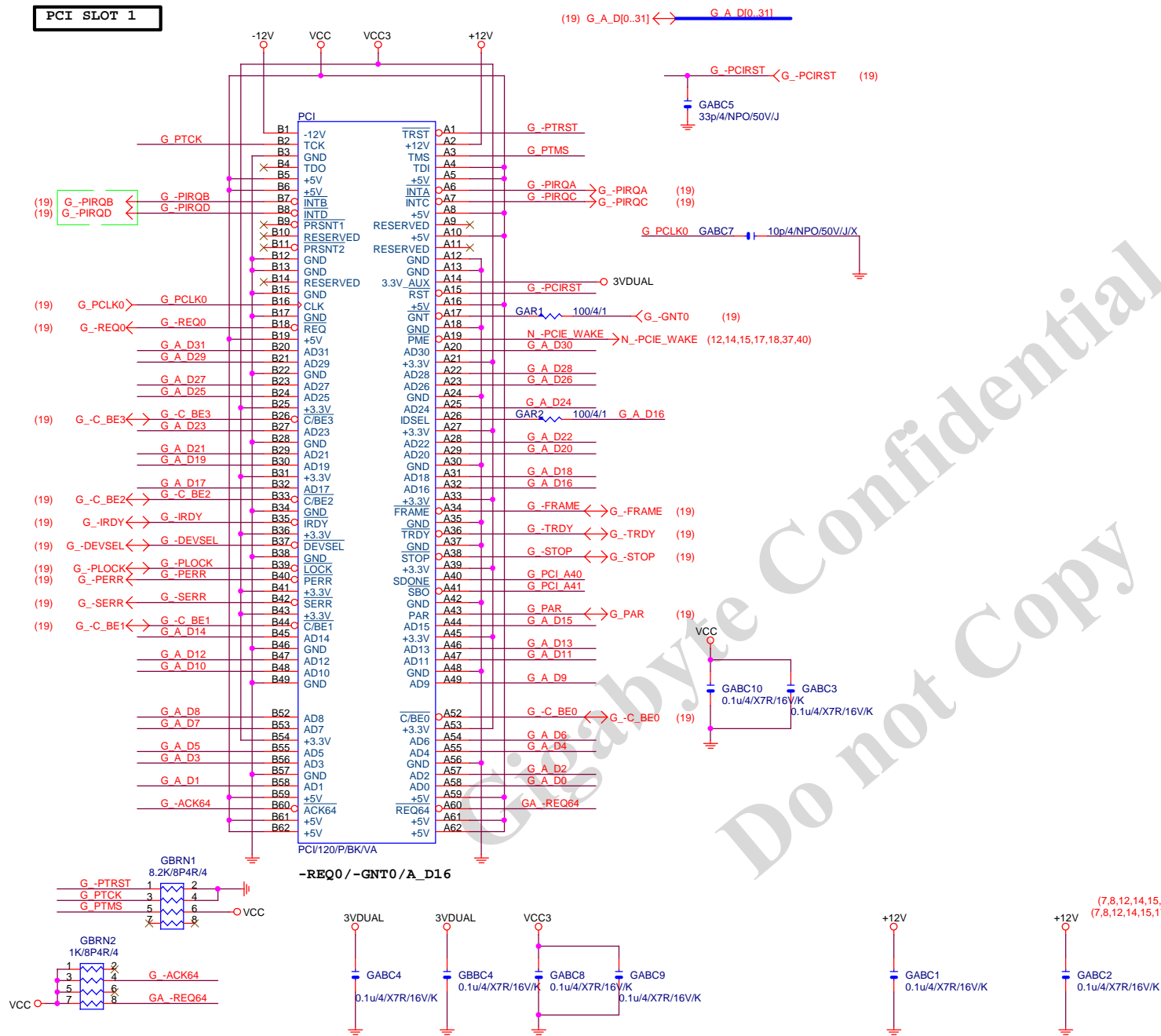
Title			
PCIE_X1 1,2,3			
Size	Document Number	Rev	
Custom	GA-Z77X-D3H	1.2	
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PCIE*4

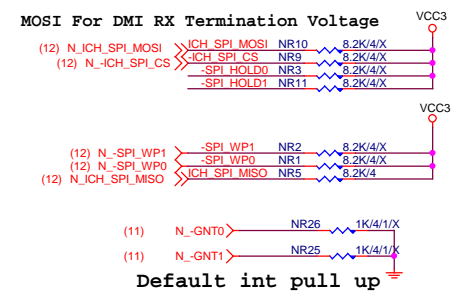
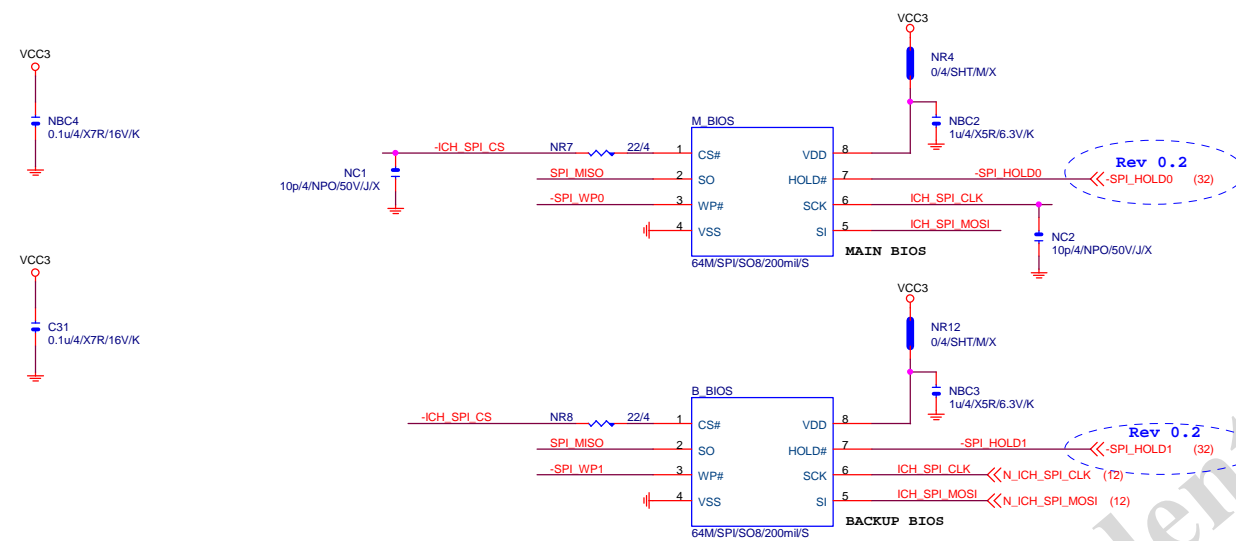




PCI SLOT 1



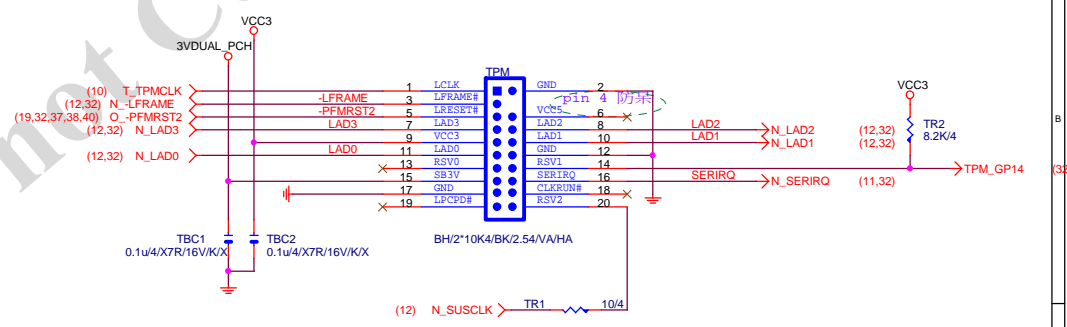
GIGABYTE™			
Title			
PCI SLOT 1&2			
Size	Document Number		Rev
Custom	GA-Z77X-D3H		1.2
Date:	Wednesday, July 24, 2013	Sheet	20 of 41



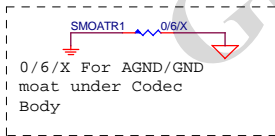
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

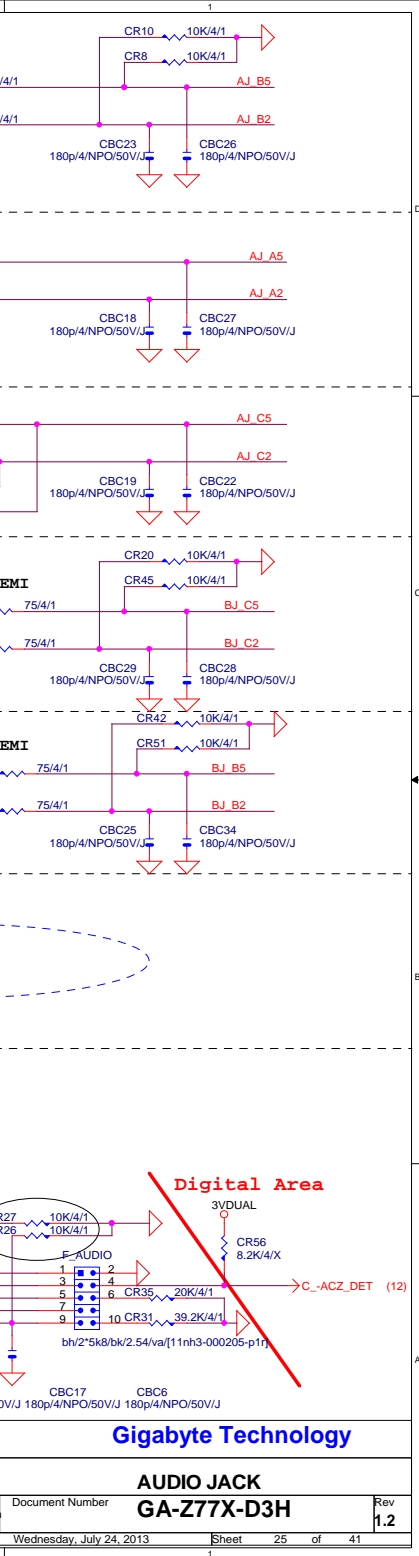
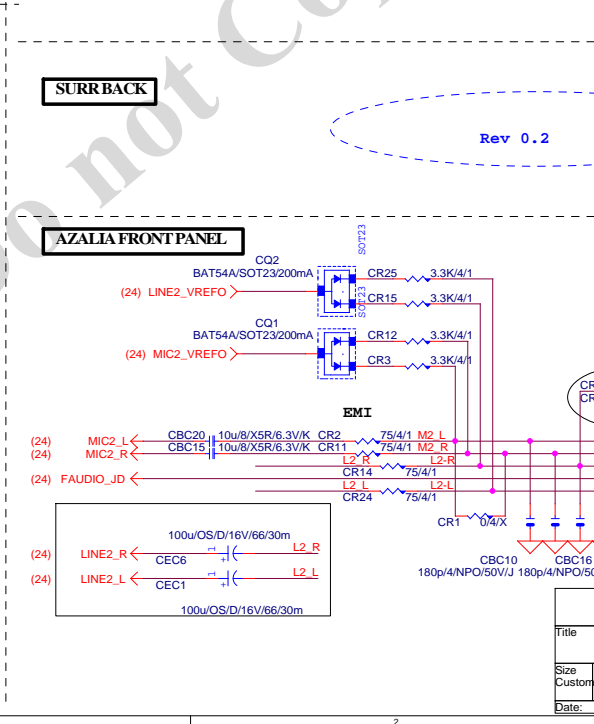
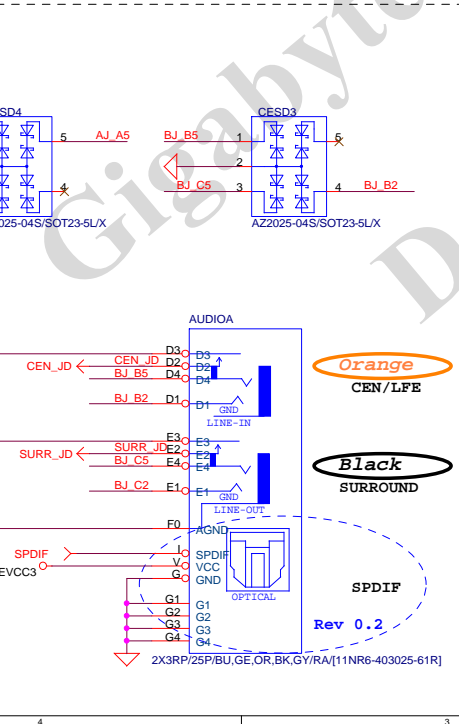
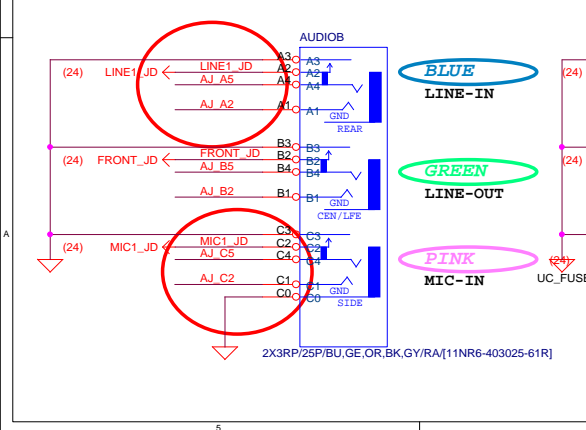
1 means floating
0 means PD 1k

Rev 0.2

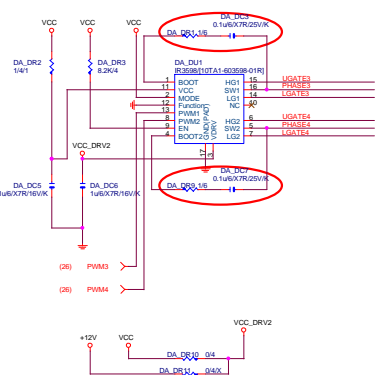


CR7/CR9/CR5/CR13/
CR29/CR32/CR46/CR19/
CR50/CR41/CR21/CR47/
CR2/CR11/CR14/CR24



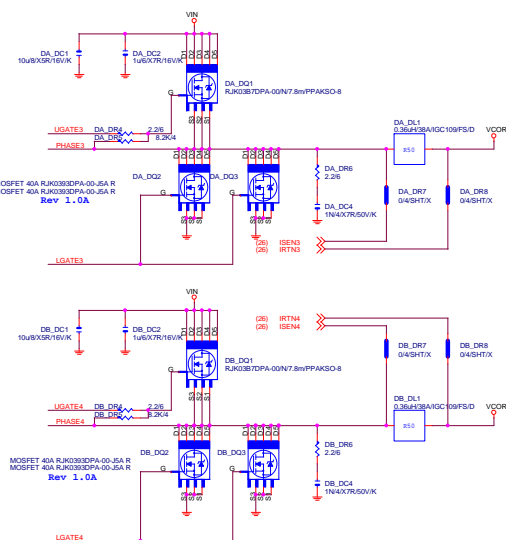


VCORE Phase 3,6

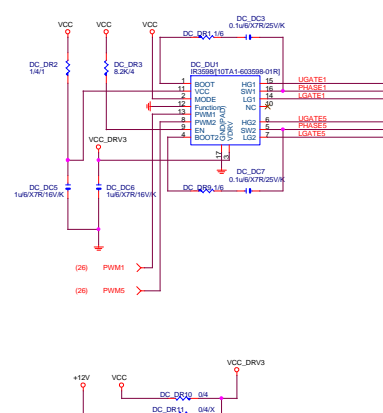


FUNCTION	MODE	PRN	MODE	PRN	MODE
1	1	1P	1P	1P	1P
2	2	2P	2P	2P	2P
3	3	3P	3P	3P	3P
4	4	4P	4P	4P	4P
5	5	5P	5P	5P	5P
6	6	6P	6P	6P	6P
7	7	7P	7P	7P	7P
8	8	8P	8P	8P	8P
9	9	9P	9P	9P	9P
10	10	10P	10P	10P	10P

In Quad mode - I2C pin10 link to I2C pin10
I2C pin10 link to I2C pin10 without PV

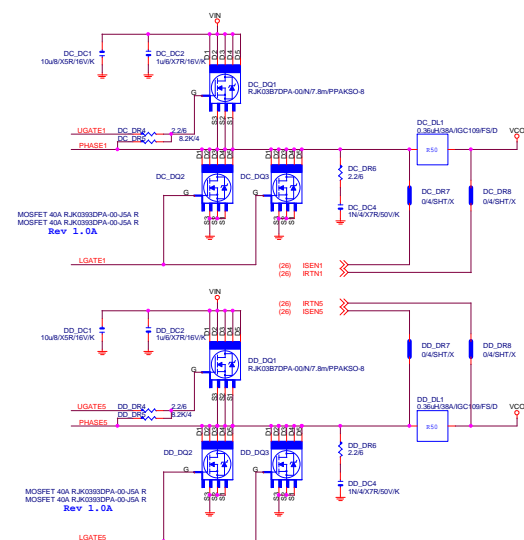


VCORE Phase 1,4

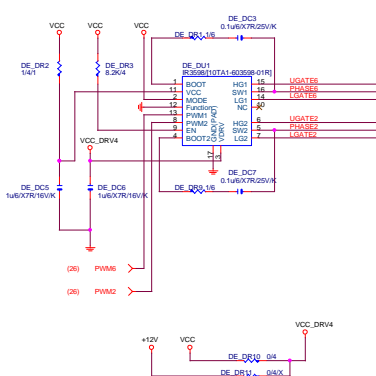


FUNCTION	MODE	PRN	MODE	PRN	MODE
1	1	1P	1P	1P	1P
2	2	2P	2P	2P	2P
3	3	3P	3P	3P	3P
4	4	4P	4P	4P	4P
5	5	5P	5P	5P	5P
6	6	6P	6P	6P	6P
7	7	7P	7P	7P	7P
8	8	8P	8P	8P	8P
9	9	9P	9P	9P	9P
10	10	10P	10P	10P	10P

In Quad mode - I2C pin10 link to I2C pin10
I2C pin10 link to I2C pin10 without PV



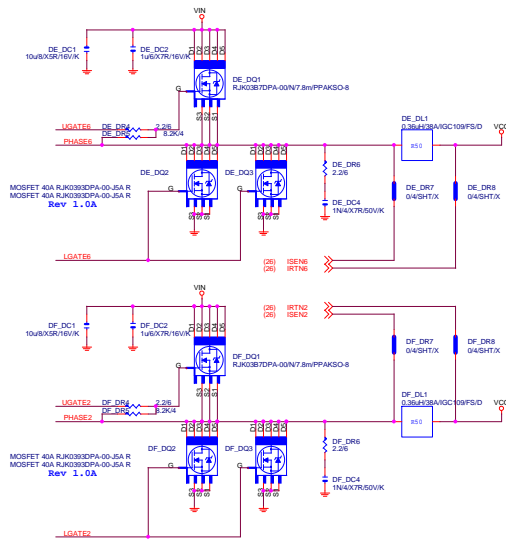
VCORE Phase 5,2



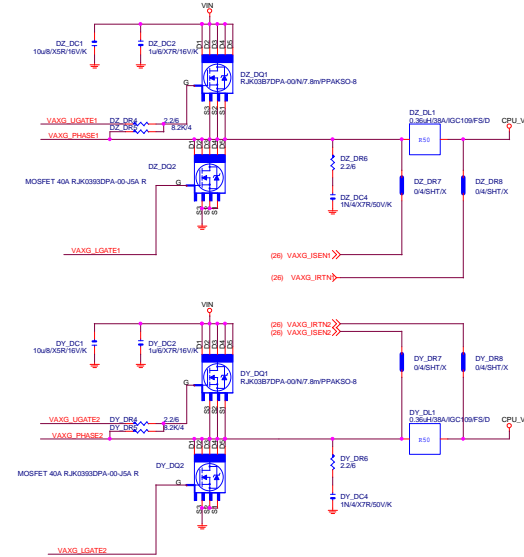
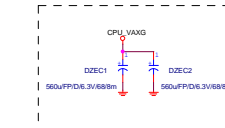
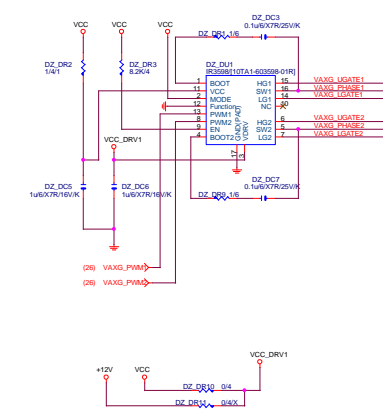
MOS HEATSINK

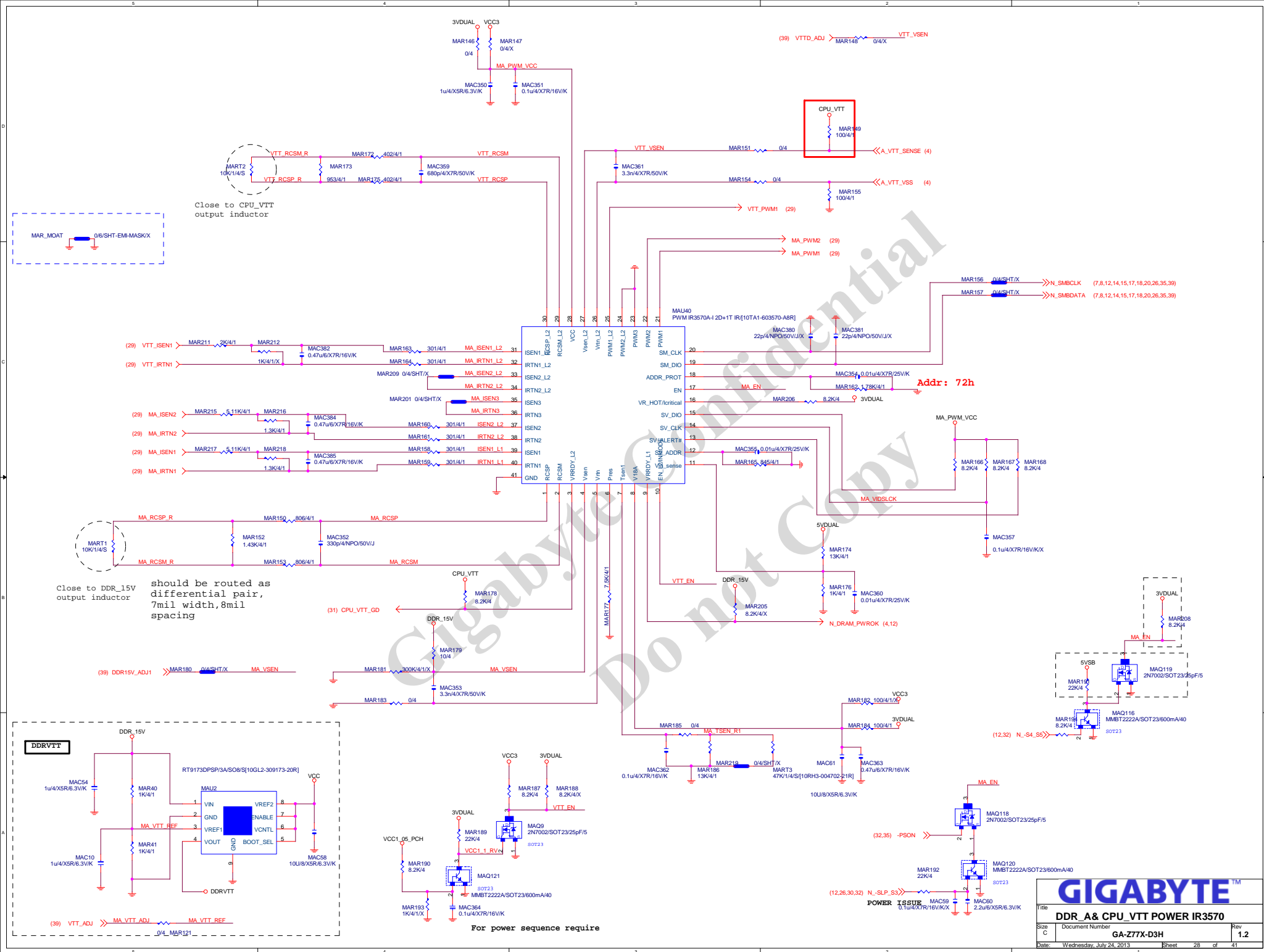


MOS HS[12SP3-S08824-01R, 12SP3-S08824-02R, 12SP3-S08824-03R]



VAXG Phase



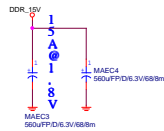
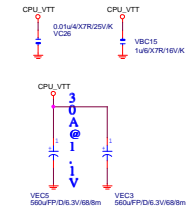
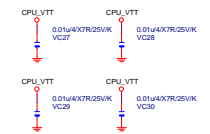
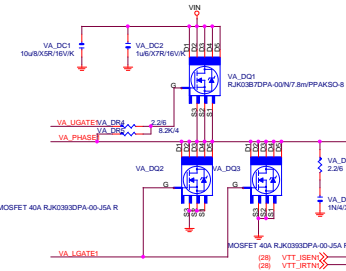
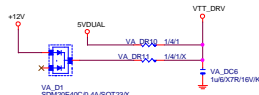


MAU1 (B360810T1-400308-01R)

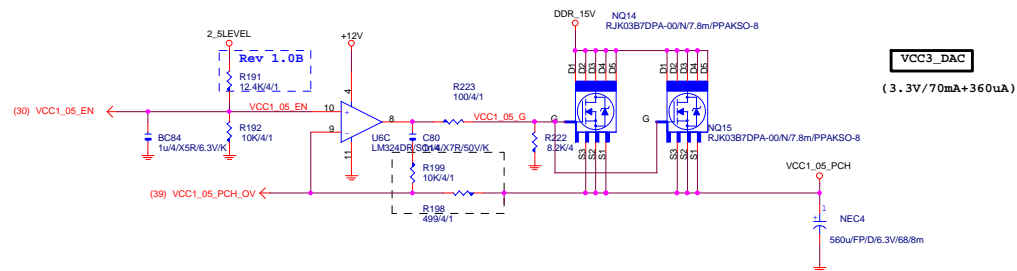
FUNCTION	MODE	PWR	MODE	MODE	MODE
0	1	18	ACTL	Double	Double
0	2	18	ACTL	Double	Double
0	3	18	ACTL	Double	Double
0	4	18	ACTL	Double	Double
0	5	18	ACTL	Double	Double
0	6	18	ACTL	Double	Double
0	7	18	ACTL	Double	Double
0	8	18	ACTL	Double	Double
0	9	18	ACTL	Double	Double
0	10	18	ACTL	Double	Double
0	11	18	ACTL	Double	Double
0	12	18	ACTL	Double	Double
0	13	18	ACTL	Double	Double
0	14	18	ACTL	Double	Double
0	15	18	ACTL	Double	Double
0	16	18	ACTL	Double	Double
0	17	18	ACTL	Double	Double
0	18	18	ACTL	Double	Double
0	19	18	ACTL	Double	Double
0	20	18	ACTL	Double	Double
0	21	18	ACTL	Double	Double
0	22	18	ACTL	Double	Double
0	23	18	ACTL	Double	Double
0	24	18	ACTL	Double	Double
0	25	18	ACTL	Double	Double
0	26	18	ACTL	Double	Double
0	27	18	ACTL	Double	Double
0	28	18	ACTL	Double	Double
0	29	18	ACTL	Double	Double
0	30	18	ACTL	Double	Double
0	31	18	ACTL	Double	Double
0	32	18	ACTL	Double	Double
0	33	18	ACTL	Double	Double
0	34	18	ACTL	Double	Double
0	35	18	ACT		

FUNCTION	MODE	FSM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Seate	DUAL
1	0	Tri-Seate	Doubler
OPEN	0	Tri-Seate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

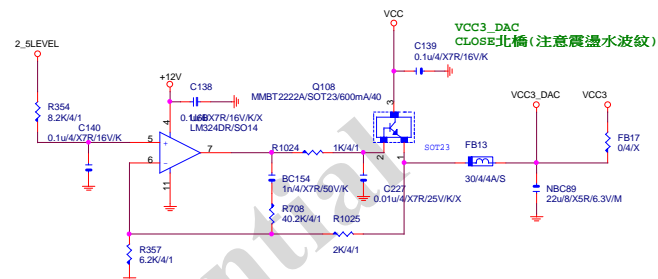
[illegible]

VCC1_05_PCH

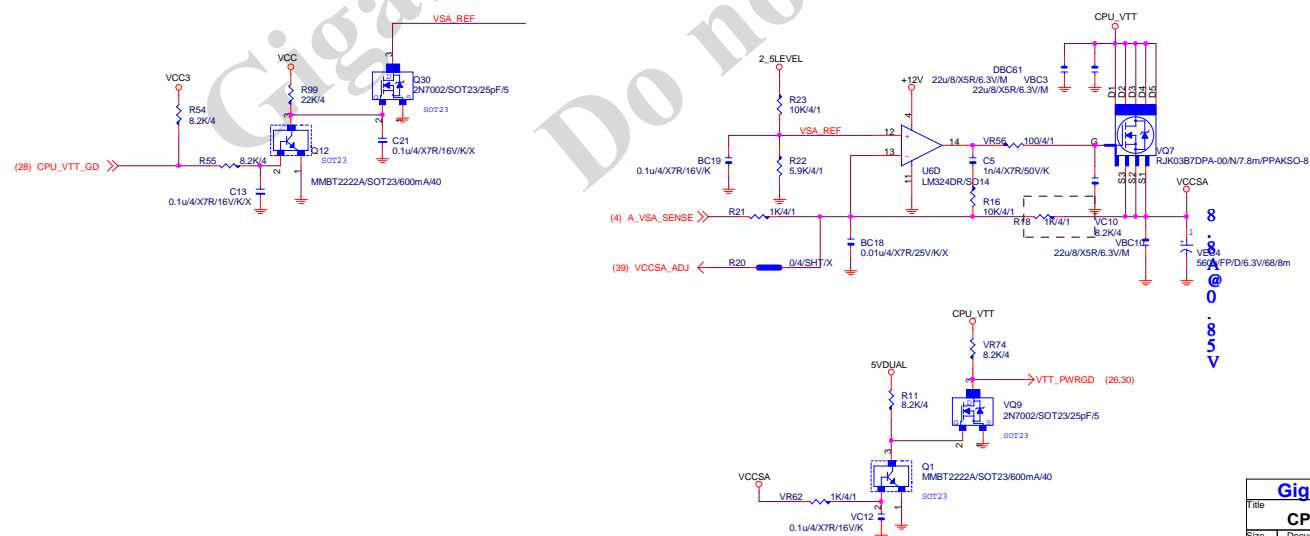


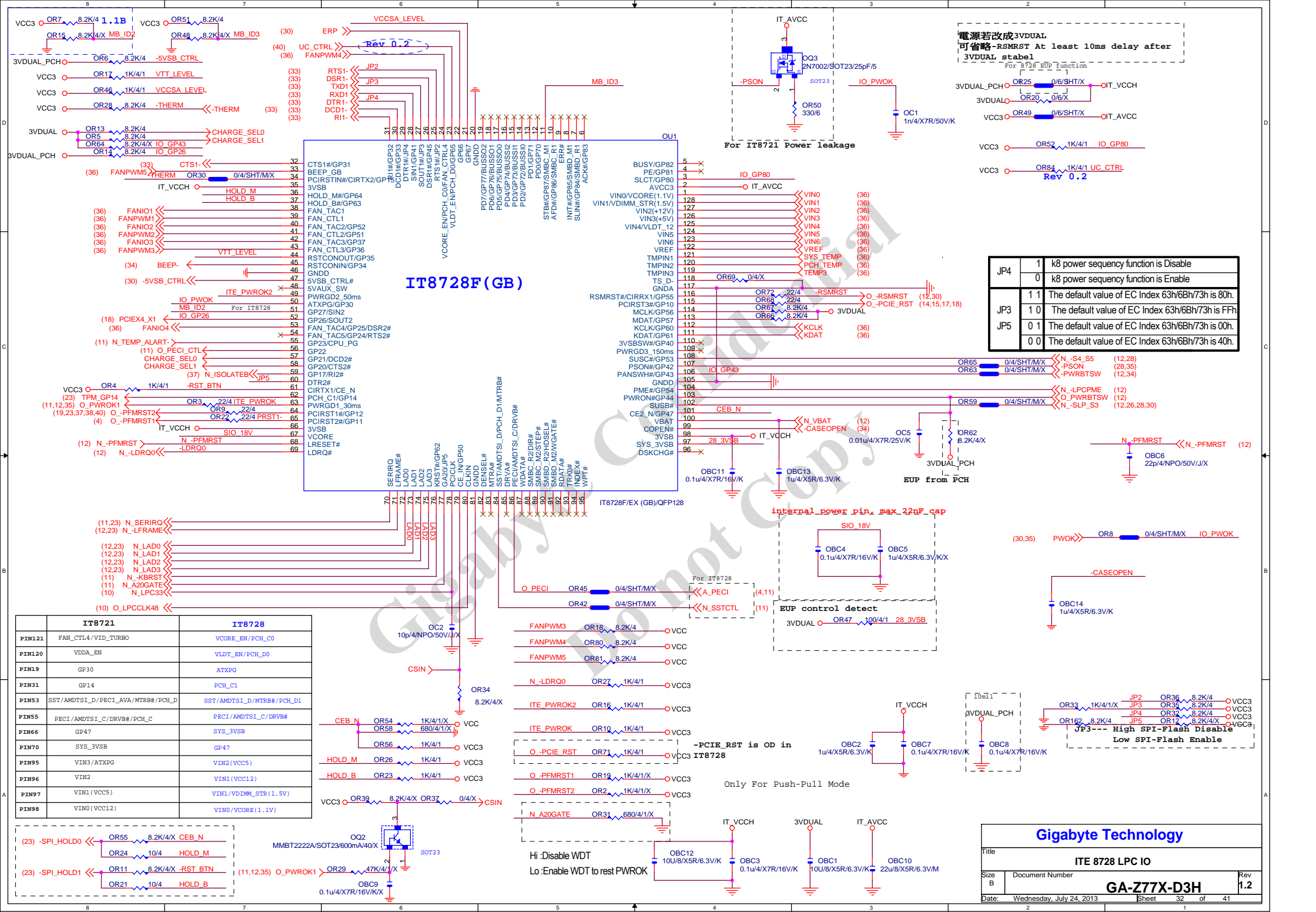
VCC3_DAC

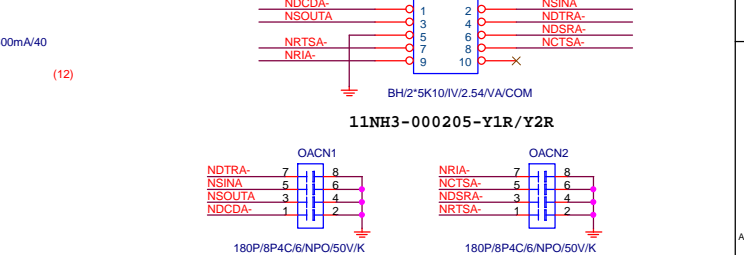
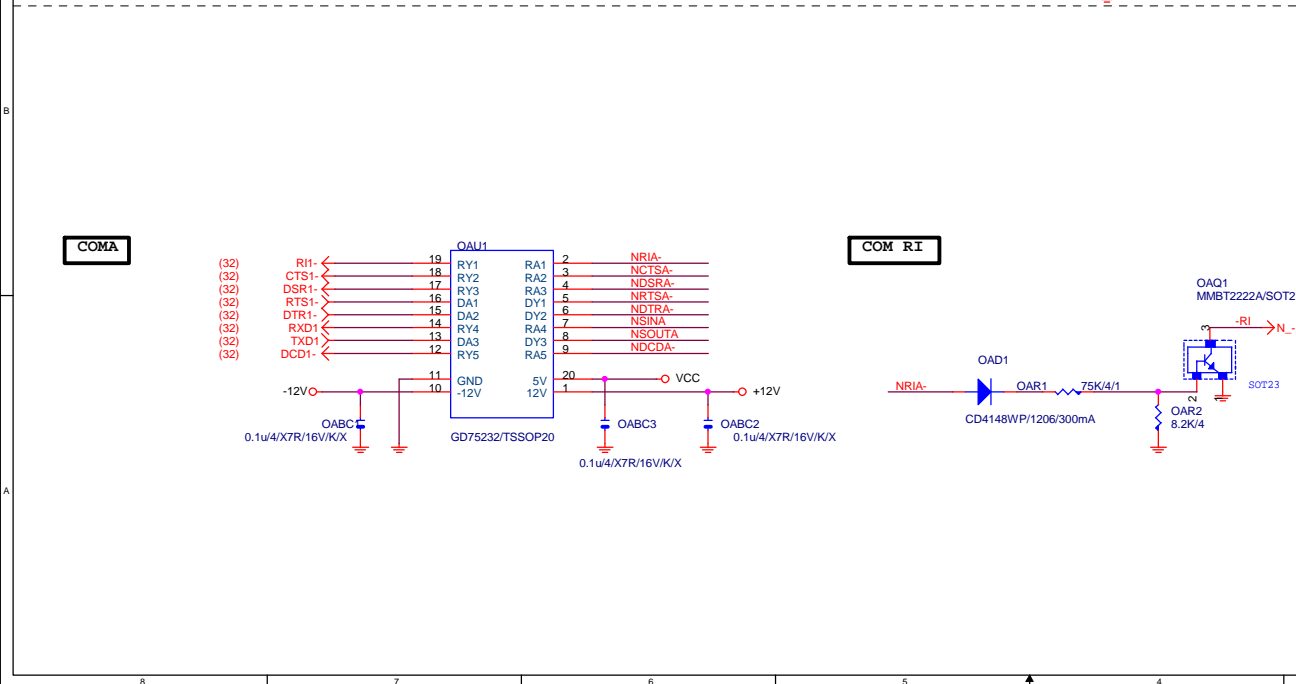
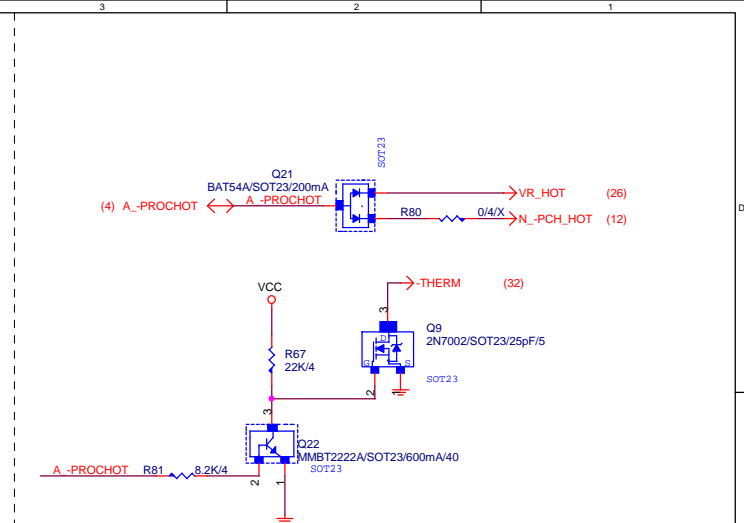
(3.3V/70mA+360uA)



VCC_SA

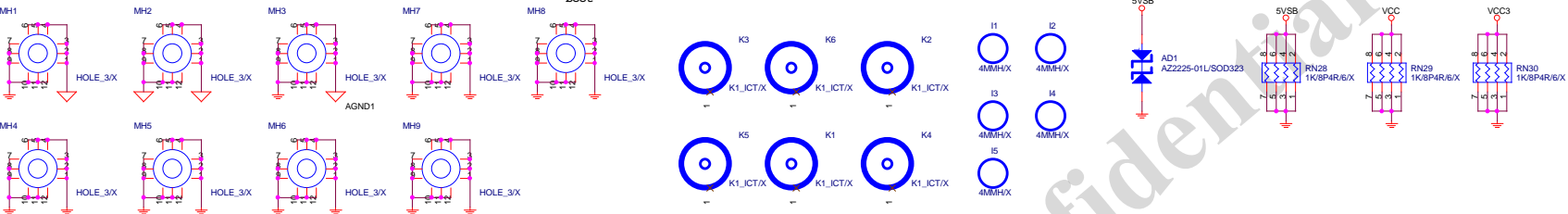






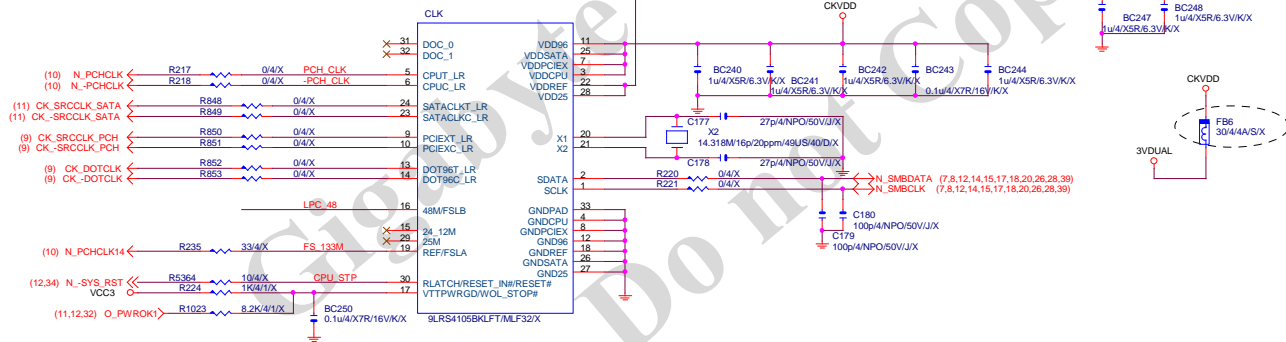
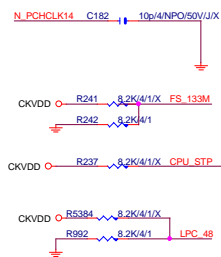
Rev 1.1

Pin	ATX	3.3V	3.3V
13	3.3V	3.3V	
14	-12V	3.3V	
15	GND	GND	
16	PSON	5V	
17	GND	GND	
18	GND	5V	
19	GND	GND	
20	-5V	POK	
21	5V	5VSB	
22	5V	12V	
23	5V	12V	
24	GND	3.3V	



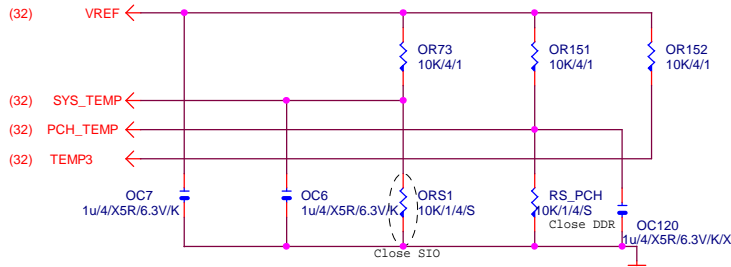
CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M

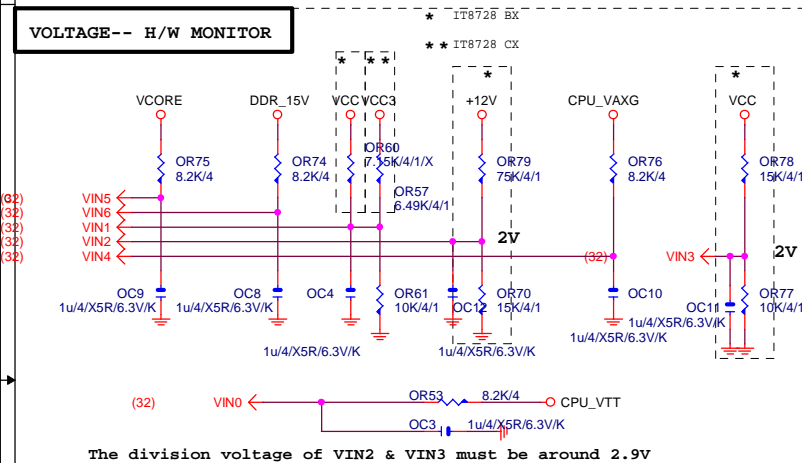


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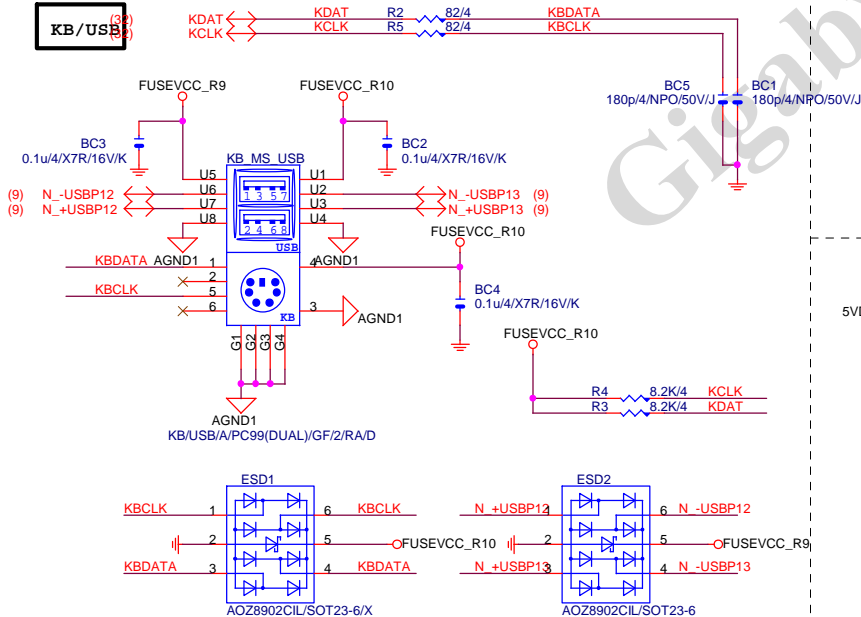
TEMP H/W MONITOR



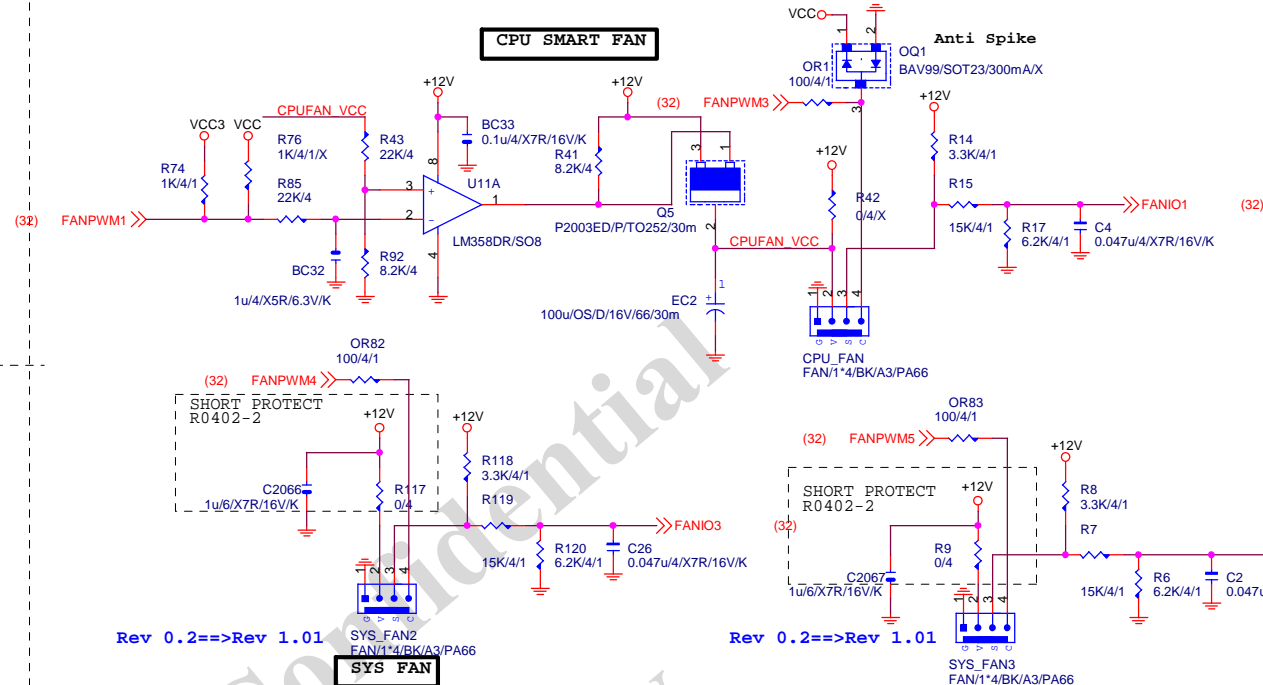
VOLTAGE-- H/W MONITOR



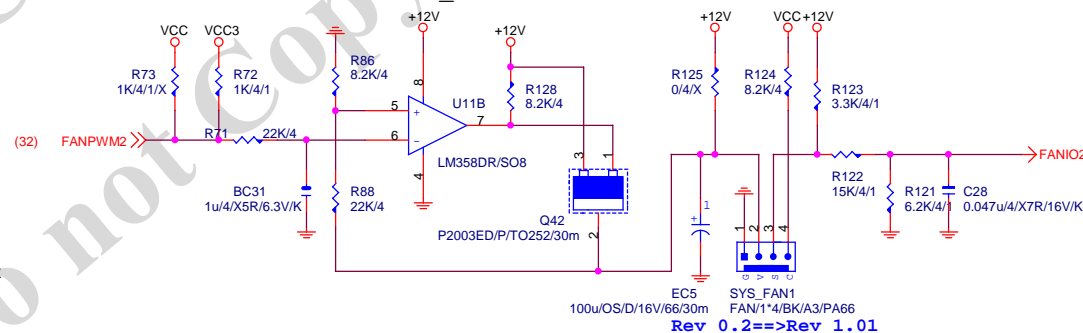
KB/USB



CPU SMART FAN

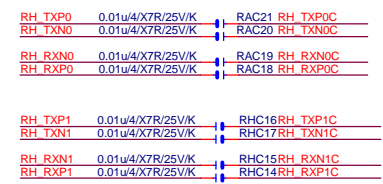
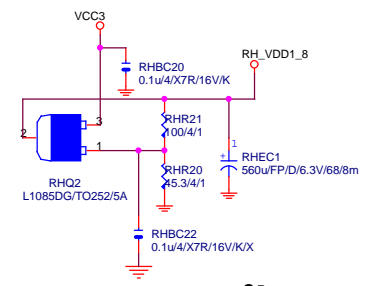
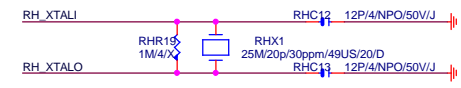
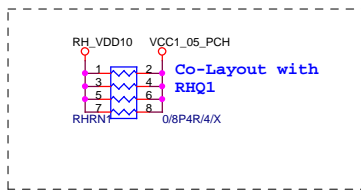
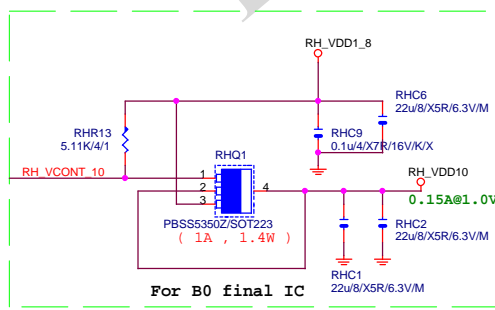
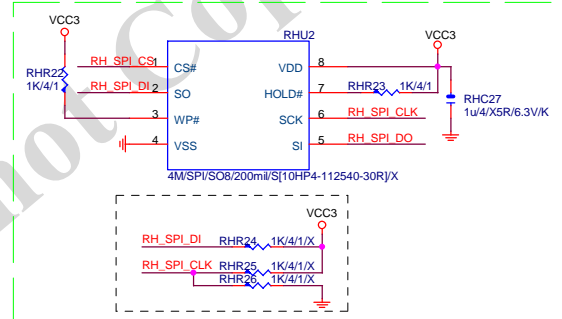
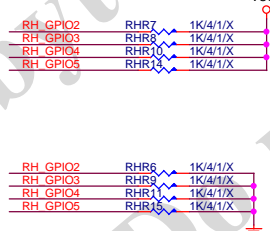
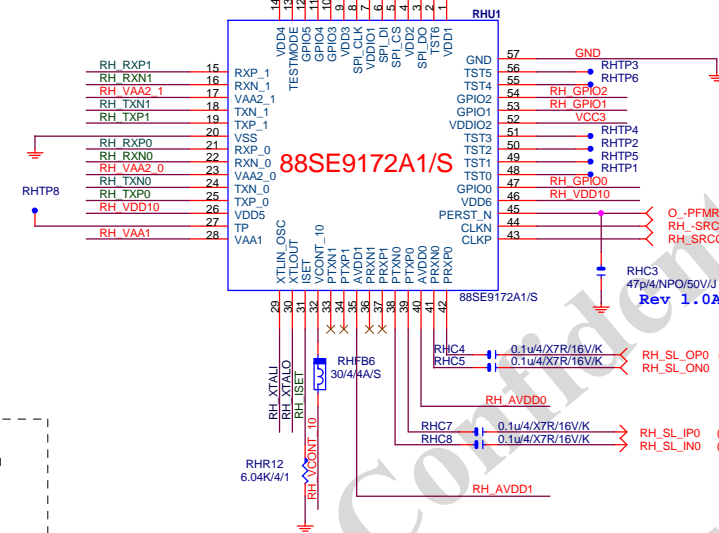
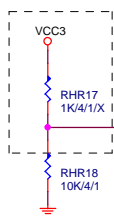
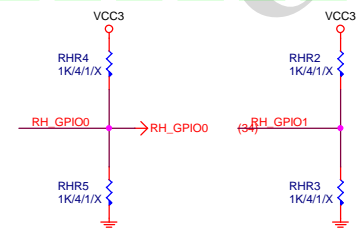
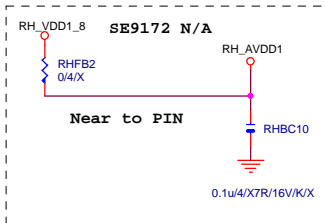
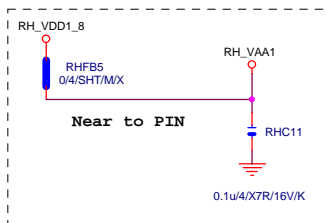
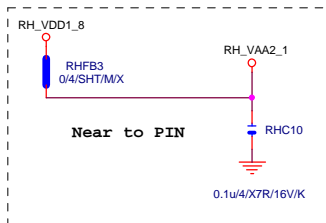
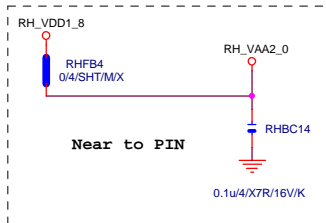
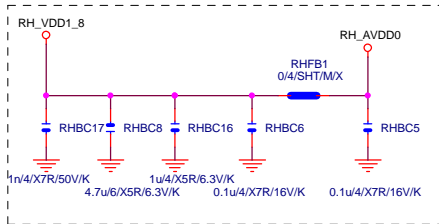
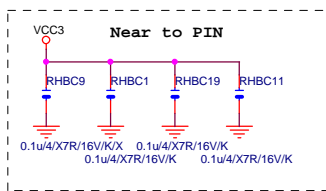
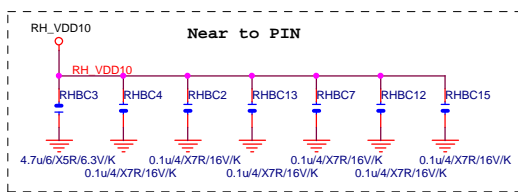


Linear SYS_FAN

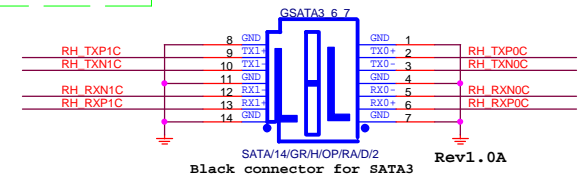


Gigabyte Technology

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